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Flexible packaging of solid-state integrated circuit chips with elastomeric microfluidics

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A flexible technology is proposed to integrate smart electronics and microfluidics all embedded in an elastomer package. The microfluidic channels are used to deliver both liquid samples and liquid metals to the integrated circuits (ICs). The liquid metals are used to realize electrical interconnects to the IC chip. This avoids the traditional IC packaging challenges, such as wire-bonding and flip-chip bonding, which are not compatible with current microfluidic technologies. As a demonstration we integrated a CMOS magnetic sensor chip and associate microfluidic channels on a polydimethylsiloxane (PDMS) substrate that allows precise delivery of small liquid samples to the sensor. Furthermore, the packaged system is fully functional under bending curvature radius of one centimetre and uniaxial strain of 15%. The flexible integration of solid-state ICs with microfluidics enables compact flexible electronic and lab-on-a-chip systems, which hold great potential for wearable health monitoring, point-of-care diagnostics and environmental sensing among many other applications.

Flexible electronics enables unconventional placements of electronics, sensors and actuators in conformal contact with nonflat surfaces, which are not achievable with rigid solid-state IC technology[1–5]. Significant progress has been made in the development of flexible electronic systems in the past few years. For example, state-of-the-art flexible bioelectronic systems have been attached to the human skin[2] or internal organs[3,4], and enabled real time continuous measurements of body temperature, blood pressure, and electrophysiological data such as electrocardiograms (ECGs)[3], electromyograms (EMGs)[4] and electrocorticograms (ECoGs)[5]. However, despite these advancements, current flexible electronic systems have not yet matched the high performance, low power consumption, low cost and scalability offered by traditional complementary metal oxide semiconductor (CMOS) IC technology. In addition, current flexible electronic systems rely on either organic molecules which often have low charge-carrier mobilities[6], or ultrathin inorganic semiconductor membranes which require delicate fabrication processes[7,8]. On the other hand, typical CMOS die measures in dimensions of only a few millimeters to a few centimeters square, easily attachable to common nonflat surfaces such as human bodies and aircraft surfaces with typical radii of curvature ranging from centimeters to meters. Therefore, if a packaging technology is available to integrate CMOS components onto a flexible and biocompatible substrate, great enhancements in performance can be expected for flexible electronic systems.

Another noticeable constraint on current flexible electronic systems is that they often provide only electronic and optoelectronic functionalities with little or no fluidic functions[8]. A consequence of this constraint is that current flexible bioelectronic systems can measure only limited physical parameters such as temperature, pressure and biopotentials, but not biomolecular markers in bodily fluids which are extremely important for early disease diagnosis and treatment monitoring[9]. A flexible technology allowing hybrid integration of solid state IC electronics/sensors with microfluidics can have transformative impacts on flexible bioelectronic systems by enabling previously unavailable biosensing capabilities such as continuous molecular biomarker monitoring embedded in a wearable device.

A key challenge in the flexible integration of solid state IC and microfluidics is that complex post-processing and packaging steps are often required[10], and the fabrication techniques involved are generally not compatible with flexible substrates[11]. In particular, the commonly used wire bonding structure in solid state IC packaging is intrinsically a three dimensional (3D) structure[12], which makes it extremely difficult to integrate separate microfluidic devices on top. Other packaging techniques, such as flip-chip bonding, can result in flat device surfaces, however the active surface is buried within the package and not accessible for microfluidic integration. In this

work, we propose and demonstrate a novel flexible IC/microfluidic hybrid integration and packaging method. As a demonstration, we used a single flexible PDMS substrate with dedicated microchannels filled with liquid metals to provide electrical interconnects to a CMOS chip and additional microchannels for hybrid integration with microfluidics without performing any post-processing on the CMOS die. The liquid metal used is a gallium-indium-tin eutectic alloy (also called Galinstan) that contains 68.5% gallium, 21.5% indium, and 10% tin, and melts at room temperature[13]. Compared with mercury, Galinstan is nontoxic, nonevaporative, and has a higher electrical conductivity and better wetting properties[13,14]. Similar gallium alloys have been used to fabricate on-chip coils, antennas and electrical wires for magnetic, RF and display applications[15–18]. In this work, along with liquid metal interconnects, microfluidic components are co-fabricated on the same PDMS substrate aligned with the CMOS die, allowing seamless IC/microfluidic integration and flexible packaging. Besides flexible electronics applications, we believe this technology will also prove an enabling method in the fields of CMOS hybrid microsystems, lab-on-a-chip, optoelectronics and optofluidics by providing novel functions previously difficult, if not impossible, to integrate such as heat management, magnetic coils, tunable antennas, and metallic optofluidic components on flexible substrates[19,22].

Results

Fabrication and flexible packaging of CMOS/microfluidic hybrid Microsystems. The packaging material, polydimethylsiloxane (PDMS), is a soft elastomer widely used in microfluidics, flexible electronics and micro-optics due to its low cost, easy fabrication, flexibility, biocompatibility and optical transparency[20]. Fig. 1 illustrates the fabrication and packaging procedures to produce flexible CMOS/microfluidic hybrid microsystems. The final packaged system is composed of two PDMS layers: a bottom CMOS layer and a top microfluidic layer. The process begins with the CMOS and the corresponding microfluidics layout design. The CMOS design is sent out to a commercial CMOS foundry for fabrication. The microfluidic layout is used to generate a photomask through either a commercial vendor or an in-house direct laser writer. The CMOS layer is fabricated as follows: the bare CMOS die from the commercial foundry is placed upside down on a flat silicon wafer; a small pressure (~5 Psi) is applied to the back side of the CMOS die to hold it in contact with the wafer; then previously degassed PDMS prepolymer is poured onto the CMOS die and baked at 80°C for 30 minutes; after being peeled off from the silicon wafer, the CMOS die is then embedded in a piece of flat PDMS with its active surface still exposed. The microfluidic layer is fabricated using conventional soft lithography techniques[21]. First a patterned SU8 photo-resist master mold is fabricated on a silicon wafer using photolithography. Then PDMS prepolymer is poured onto the mold and degassed in a vacuum chamber. The prepolymer is then baked at 80°C for 30 minutes. The partially cured PDMS is peeled off from the mold forming the microfluidic layer, and the liquid inlet/outlet ports are punched through the whole layer. For each different CMOS layout, a different mold is needed to fabricate the corresponding microfluidic layer. However, the finished master molds can be reused many times, thus reducing the fabrication cost and time. Both the CMOS and microfluidic layers are treated with oxygen or air plasma in order to form a strong bond between the two layers. Then the microfluidic layer is aligned on top of the CMOS layer to form a permanent bond. Afterward, the package is baked at 80°C overnight (or for longer than 8 hours). Finally, liquid metal Galinstan is filled into some of the microfluidic channels to form electrical interconnects to the CMOS IC. The whole process doesn't not involve harsh chemicals or high temperatures that might damage the CMOS device. It is, however, important to avoid water moisture between Galinstan and the CMOS pads because water can react with the Aluminum pads in the presence of Gallium to generate $Al(OH)_3$ and Hydrogen gas[23]. One potential issue is the corrosion problem caused by gallium on the aluminum pads which fortunately didn't cause noticeable performance degradation in our experiments. Further discussion on this issue is given in the supplementary information.

Liquid metal interconnects and microfluidic sample delivery. A photograph of the packaged CMOS and microfluidics integrated

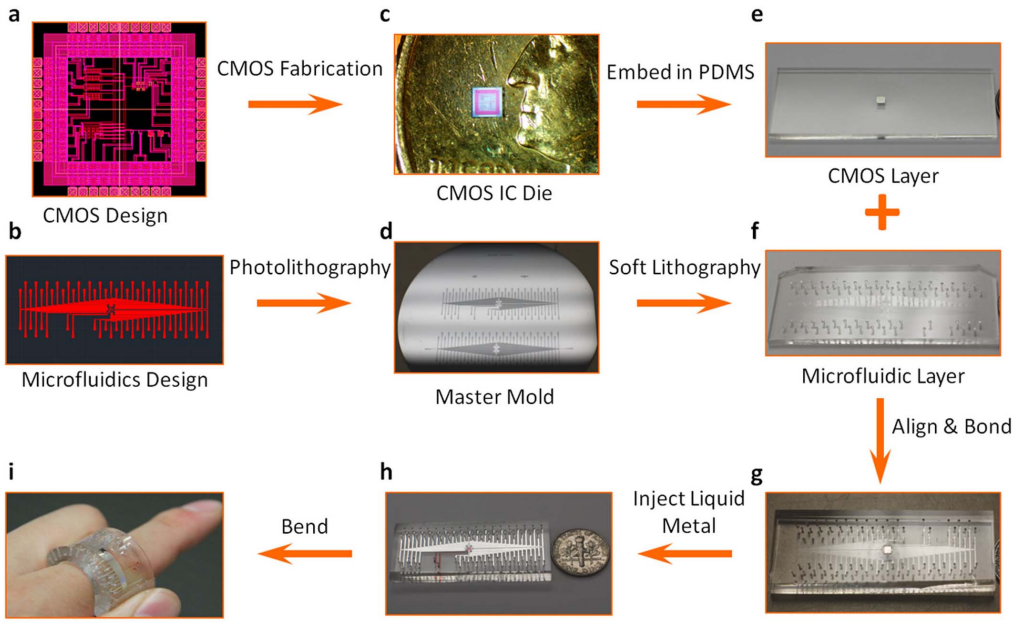

Figure 1 | Schematic illustration of the fabrication and packaging procedures to produce flexible CMOS/microfluidic hybrid microsystems. (a): CMOS layout design. (b): Microfluidics layout matched to the CMOS layout. (c): CMOS IC die fabricated by a commercial CMOS foundry. (d): SU8 master mold on a silicon wafer fabricated by photolithography. (e): CMOS layer - a CMOS die embedded in a flat PDMS layer with its active surface exposed. (f): Microfluidic layer with access holes. (g): Microfluidic layer and CMOS layer are aligned and bonded after O_2 plasma treatment. (h): Fully packaged system with liquid metal interconnects and microfluidic channels. (i): Bendable package conformally attached to a human index finger.

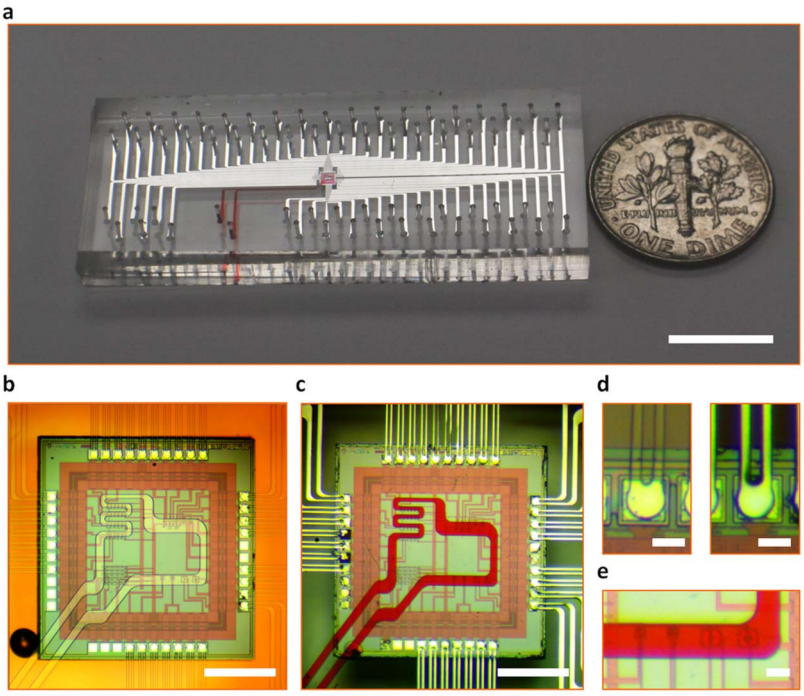

Figure 2 | Liquid metal interconnects and microfluidic sample delivery in the packaged CMOS/microfluidic hybrid microsystem. (a): Optical image of the packaged CMOS/microfluidic integrated system. (b) Optical micrograph showing the microfluidic channels are aligned with CMOS pads and sensors. (c) Optical micrograph showing the interconnect channels are filled with liquid metal and the microfluidic sample delivery channel is filled with red food dye. (d): Optical micrograph of an interconnect channel aligned with a CMOS contact pad before (left) and after (right) liquid metal is injected. (e): A microfluidic channel is accurately aligned with the sensor area. Scale bars: (a) 1 cm; (b) 500 μm; (c) 500 μm; (d) 50 μm; (e) 50 μm.

system is shown in Fig. 2a. The thickness of the whole package can vary from 1.5 mm to 5 mm, depending on the amount of PDMS used. Thinner devices are more flexible. The footprint of the whole package is about 2 cm by 5 cm when using a 40 pad CMOS chip. This footprint is limited by the number of input/output (I/O) ports that are needed to inject liquid metals to make electrical connections. The size of each (I/O) port is about 750 μm in diameter and must be separated from each other by about 1 mm. However, for applications

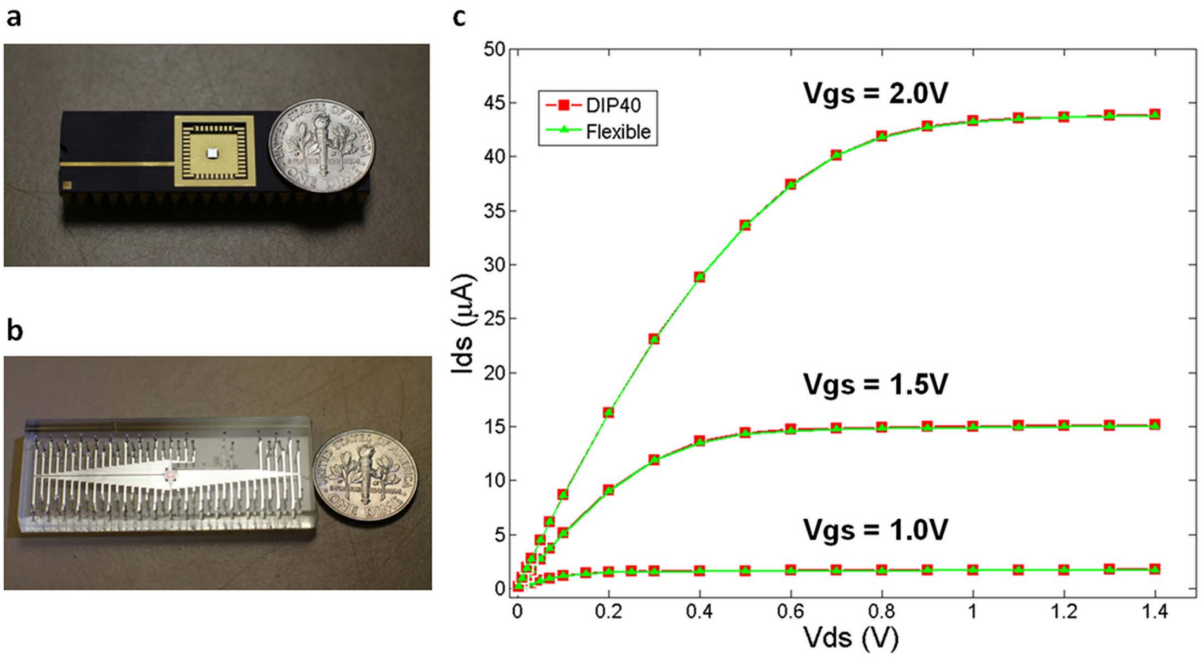

Figure 3 | Measured Ids-Vds characteristics of NMOS transistors in conventional DIP and flexible packages. (a): The CMOS chip in a conventional DIP-40 package, (b): The CMOS chip in a flexible PDMS package with liquid metal interconnects. (c): Measured I–V curves of the NMOS transistors in the two different packages showing excellent agreements between each other. Error bars are included and have been computed as the standard deviation of five independent measurements, however they are not visually discernible as the typical standard deviation is less than 1% of the measured value.

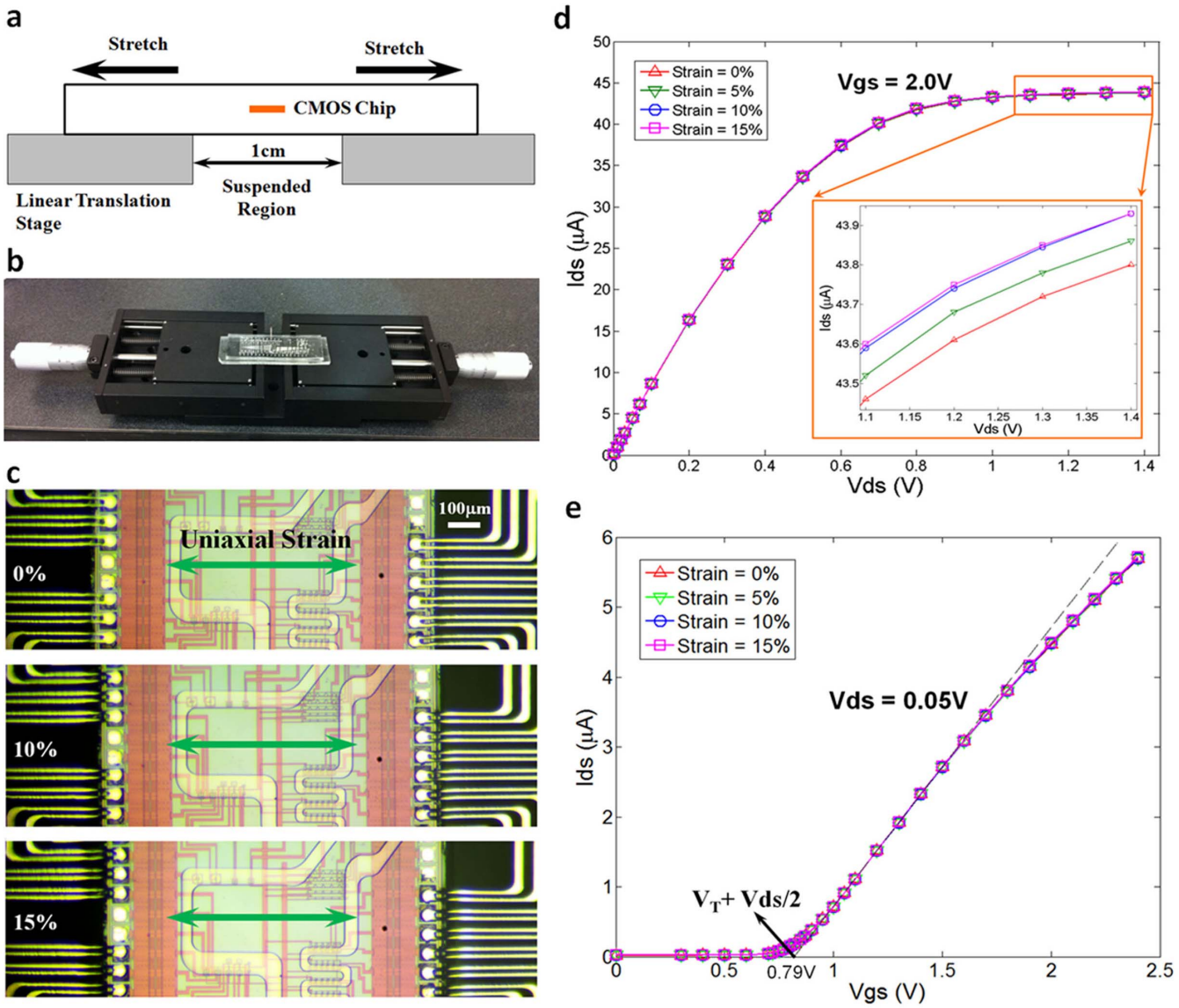

Figure 4 | Measured I–V characteristics of an NMOS transistor in the flexible packages under different uniaxial stretching conditions. (a): Schematic showing the measurement setup. The central suspended region of the package is 1 cm long. (b): Photograph of the real setup showing the package was glued to two linear translation stages. (c): Optical micrographs of the CMOS chip in the package under different uniaxial strains. It can be seen that most of the strain was in the PDMS/Liquid metal region. (d): Measured $I_{ds}-V_{ds}$ curves of the NMOS transistor under different linear strains showing excellent agreements among each other. (e): Measured $I_{ds}-V_{gs}$ curves of the NMOS transistor under different linear strains. The linearly extrapolated threshold voltage V_T is 0.765 V. Error bars are included and have been computed as the standard deviation of five independent measurements.

such as wireless sensing where the power source and I/O components are fully integrated in the package, such I/O ports are not needed and the final package size can be much smaller. At the center of the packaged device, a CMOS die of 1.5 mm by 1.5 mm in size is embedded. As shown in Fig. 2b, microfluidic channels aligned with the contact pads on the CMOS die are filled with Galinstan to allow electrical connections to the CMOS circuits while a separate microchannel is used for liquid sample delivery to the sensor area. Previously, we have used Galinstan to fabricate on-chip microphotonic components integrated with PDMS microfluidics[22]. Our experiences showed that Galinstan can be injected into microchannels as small as 4 μm wide and 2 μm high. More detailed information on Galinstan is given in the supplementary information.

Small stainless steel tubes can be plugged into the access holes to inject liquid metal. After liquid metal was filled into the channels, the stainless steel tubes were left in the holes to facilitate electrical connections to the test equipments. As shown in Fig. 2b & c, 32 microfluidic channels were accurately aligned with the corresponding CMOS pads. Each channel also has a venting port to avoid high pressure buildup during liquid metal injection. The pad size in our CMOS chip design is 80 μm by 80 μm with 15 μm gap between pads. So the microfluidic channels were designed with a 50 μm diameter tip. The channels connected with the tip are as narrow as 15 μm in width and 20 μm in height. As the channels move away from the tip, the width of the channels is increased to larger values (50 μm and 100 μm) for smaller electrical resistance of the interconnection. The measured resistivity of Galinstan is $(2.85\pm0.09)\times10^{-7}\Omega\cdot$m and the total resistance due to liquid metal is between 5Ω and 15Ω depending on the length of the channel. The alignment accuracy was ±5 μm using manual alignment under a 180X magnification stereoscope. If needed, mask aligners can be used to achieve sub-micron alignment accuracy. Fig. 2d shows the liquid metal contacting a CMOS pad. An

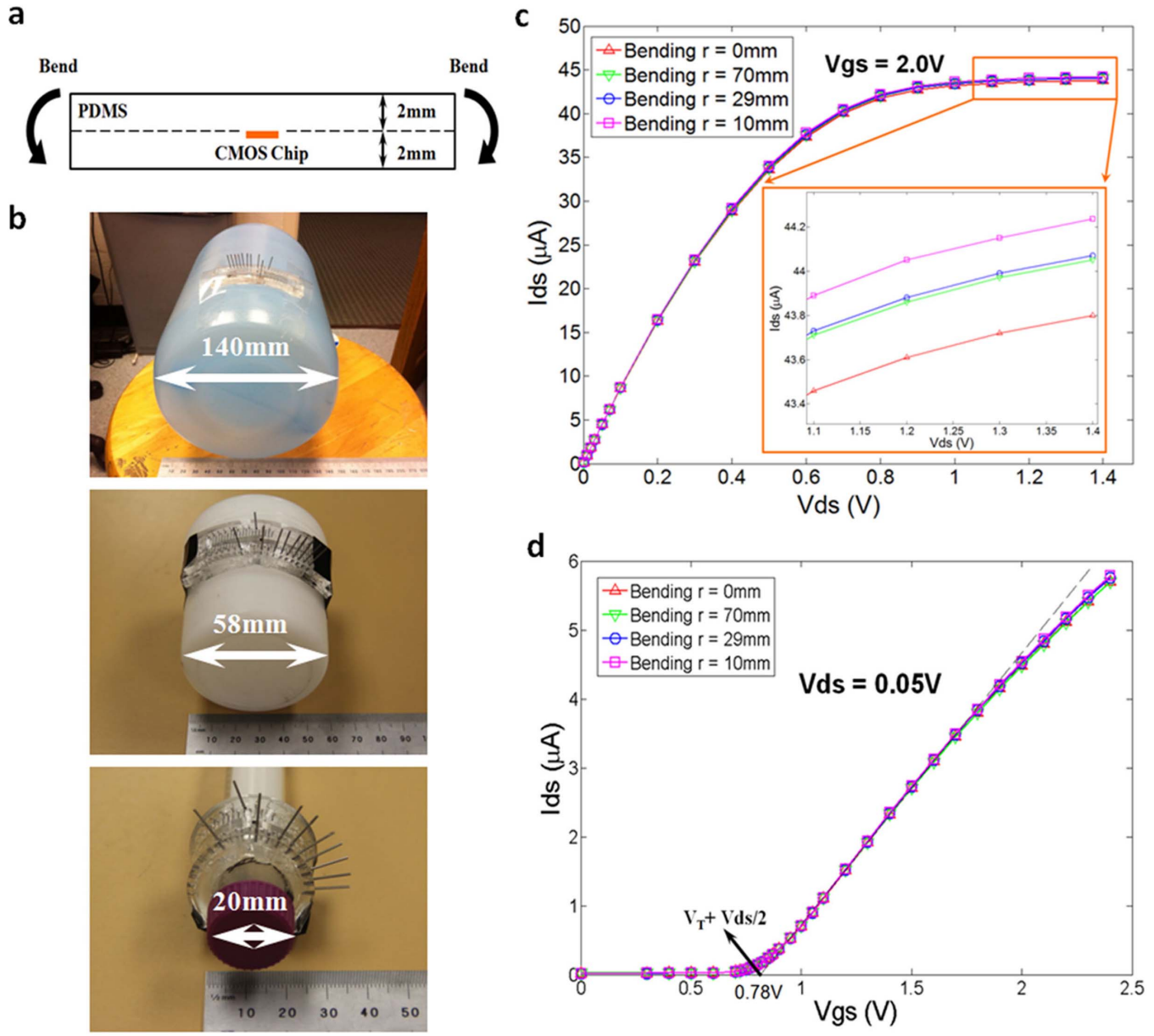

Figure 5 | Measured I–V characteristics of an NMOS transistor in the flexible packages under different bending conditions. (a): Schematic showing the measurement geometry. The CMOS chip is located near the neutral mechanical plane. (b): Photographs showing the package was conformally attached to cylindrical tubes with diameter from 140 mm to 20 mm. (c): Measured $I_{ds}-V_{ds}$ curves of the NMOS transistor under different bending radii. (d): Measured $I_{ds}-V_{gs}$ curves of the NMOS transistor under different bending radii. The linearly extrapolated threshold voltage V_T is 0.755 V. Error bars are included and have been computed as the standard deviation of five independent measurements.

additional 70 μm wide microfluidic channel is aligned with the CMOS sensor area for accurate liquid sample delivery, as highlighted by a red food dye shown in Fig. 2c & 2e.

I–V characterization of NMOS transistors with liquid metal interconnects. To verify the liquid metal interconnection, the contact pads of an enhanced-mode NMOS transistor (channel width W = 5 μm, channel length L = 10 μm) on a CMOS chip were connected using liquid metals. The NMOS transistor was designed in a 0.5 μm CMOS technology and fabricated by the On Semiconductor C5 0.5 μm CMOS process. As shown in Fig. 3c, the drain current vs. drain-to-source voltage ($I_{ds}-V_{ds}$) curve of the transistor was successfully measured. The NMOS transistor was connected in a common source configuration and the gate voltage was set at fixed values (V_{gs} = 1.0 V, 1.5 V and 2.0 V). The drain voltage V_{ds} was swept from 0 V to 1.4 V and the drain current I_{ds} was recorded. For comparison, the $I_{ds}-V_{ds}$ curve of another NMOS transistor was also measured with the same design parameters and from the same fabrication process but packaged in a traditional dual-in-line 40 (DIP-40) package. The measured drain currents of the liquid metal connected transistor differed less than 1% from those of the DIP-40 packaged transistor.

I–V characterization of an NMOS transistor in the flexible package under different stretching conditions. In order to verify the package flexibility we also tested the transistor I–V characteristics when the package is under different uniaxial stretching conditions. The package was glued to two high resolution linear translation stages with a 1 cm long suspended region in the middle as shown in Fig. 4a&b. Fig. 4d shows the measured $I_{ds}-V_{ds}$ curve of the

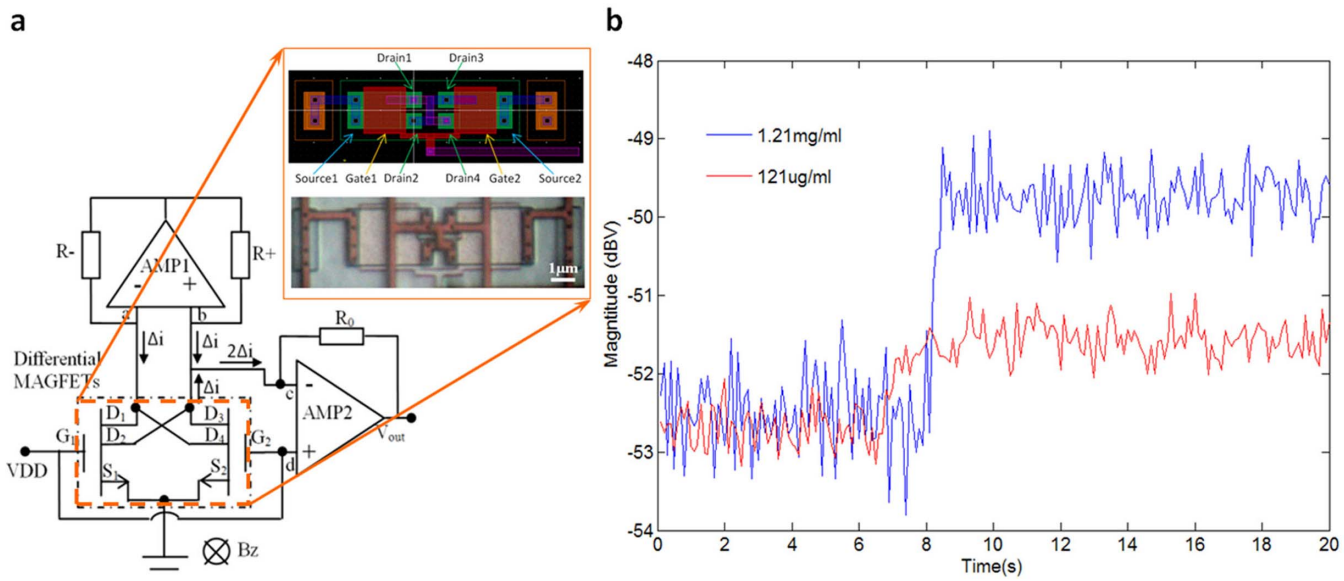

Figure 6 | Detection of magnetic nanoparticles in water with a packaged CMOS MAGFET/microfluidic hybrid microsystem. (a): CMOS MAGFET readout circuit[27]. Inset shows the design layout and optical micrograph of the MAGFET. Scale bar: 1 μm. (b): Detection of magnetite nanoparticles in water using the packaged CMOS/microfluidic hybrid microsystem.

transistor and Fig. 4e shows the measured $I_{ds}-V_{gs}$ curve. For the $I_{ds}-V_{gs}$ measurements, the NMOS transistor was biased at a low drain voltage V_{ds} = 0.05 V and the gate voltage V_{gs} was swept from 0 V to 2.4 V. The transistor remained fully functional under uniaxial strains up to 15% over the 1 cm suspended region, and the measured drain currents differed less than 0.5% from those of the flat PDMS package. We also observed slight variations in drain currents (less than 0.4%) when the strain was increased from 0% to 15% (Fig. 4d). The linearly extrapolated threshold voltage V_T was 0.765 V which agrees well with the foundry provided data (between 0.70 V and 0.83 V depending on channel dimensions[24]). The highly reproducible device performance is partially contributed by the fact that the Young's modulus of Silicon (~130 to 170 GPa depending on orientation relative to the crystal lattice[25]) is five orders of magnitude higher than that of PDMS (~1.5 MPa for RTV 615[26]). Therefore, as can be seen in Fig. 4c, most of the strain is in the PDMS (and liquid metal) region of the package and the mechanical strain on the CMOS chip is quite small which is beneficial for stable device performance under stretching conditions.

I–V characterization of an NMOS transistor in the flexible package under different bending conditions. We also measured the transistor I–V characteristics when the package is under different bending conditions. The package was conformally attached to a cylindrical tube with a radius ranging from 70 mm to 10 mm as shown in Fig. 5b. In the tested package, both the top and bottom PDMS layers are 2 mm thick and therefore the CMOS die is located near the neutral mechanical plane. The NMOS transistor remained fully functional under bending radius of 10 mm, and the measured drain currents differed less than 1.5% from those of the flat PDMS package as shown in Fig. 5c&d. The smallest bending radius at which we have observed functional transistors is 7.5 mm. However, at a bending radius of 7.5 mm, some of the electrical interconnects became less stable and a few were broken. The instability or failure is not due to damage to the CMOS die because after repackaged into a new device, the CMOS die was still fully functional. Further experiments are needed to determine the exact cause for the broken connections. If higher mechanical flexibility is required for the CMOS die, chemical mechanical polishing (CMP) can be used to thin the die from the current 250 μm to below 50 μm.

Detection of magnetic nanoparticles in solution using a CMOS MAGFET/microfluidic hybrid microsystem. Most state-of-the-art CMOS/microfluidic hybrid systems rely on complex post-processing on the CMOS die[10,27] or use only simple microfluidic reservoirs. As a demonstration of the proposed packaging technology, we integrated a CMOS magnetic sensor chip with a PDMS microfluidic sample delivery channel without performing any post-processing on the CMOS die. The CMOS magnetic sensor is a split-drain Hall effect magnetic field-effect transistor (MAGFET)[28]. When a MAGFET is exposed to a magnetic field, current deflection will produce an imbalance of the two drain currents due to the Hall effect[28]. In our experiments, a differential MAGFET design was used to further improve the sensitivity[29]. The MAGFET was designed in a 0.5 μm CMOS technology and fabricated by the On Semiconductor C5 0.5 μm CMOS N-well process. A more detailed description of the used MAGFET can be found in Ref. 28. Magnetite Fe_3O_4 nanoparticles in water with different concentrations (121 μg/mL and 1.21 mg/mL) were inject (under 2 Psi pressure) into the microfluidic channel above a MAGFET detector on the CMOS chip. A Helmholtz coil was used to generate a 60Gauss polarization magnetic field applied on the MAGFET and the magnetic nanoparticles[30]. The detailed experimental setup is given in supplementary Fig. S6. The CMOS MAGFET readout circuit is shown in Fig. 6a[31]. The measured MAGFET output signals are shown in Fig. 6b. When a 121 μg/mL magnetic nanoparticle solution is flowed across the CMOS sensor area, the output signal increased by about 1 dBV. This is, to our knowledge, the first experimental demonstration of a fully integrated CMOS/microfluidic hybrid microsystem without performing any wire bonding or post-processing on the CMOS die.

Discussion

The flexible IC/microfluidic integration and packaging technology reported here enables the seamless integration of CMOS sensor chips with PDMS microfluidics, thus achieving a true lab-on-a-chip system that have both CMOS functionalities and microfluidic sample manipulation on the same flexible substrate. By integrating PDMS microfluidics with CMOS sensor chips, a number of additional advantages can be obtained compared with traditional biosensor devices where fluidics and sensor device are decoupled. For example, by using active fluidic flow and reducing the distances

between target molecules and sensor surface, more efficient and faster molecular binding can be achieved, which can improve both the detection sensitivity and throughput. In the case of CMOS optical sensors, by using a shallow channel, we can not only obtain high photon collection efficiency and reduced background, but also eliminate the complex and bulky optics used in conventional optical sensing configurations. In addition, by combining CMOS actuators/electronics with PDMS valves[32,33], fully integrated on-chip valves and pumps may become possible without relying on any external pressure sources. Such self-contained compact IC/microfluidic hybrid microsystems can find many applications in point-of-care diagnostics, environmental monitoring and food safety inspection applications. The flexible integration of solid state IC electronics, sensors and microfluidics also holds great potential for wearable wireless monitoring of human health where real-time and continuous health/wellbeing data can be obtained and wirelessly communicated to the doctor or a central database for accurate and timely interpretation.

Methods

Microfluidics layout design. The microfluidics layout was designed for a 1.5 mm by 1.5 mm CMOS die with 40 contact pads and an array of MAGFET sensors. The microfluidic channels need to match the positions and size of the CMOS pads. In addition the microfluidic sample delivery channel needs to match the positions and sizes of the CMOS MAGFET sensors. Due to the shrinkage (about 1.5%) of PDMS after curing, small expansion of the layout size was introduced in the design file (AutoCAD) to mitigate this effect. The detailed microfluidics layout design of the mold is shown in supplementary Fig. S3.

Fabrication and packaging of flexible CMOS/microfluidic hybrid Microsystems. The SU8 master mold for the microfluidic layer was fabricated on a 3 inch silicon wafer using *i*-line photolithography. 20 μm thick SU8 (SU8-3010 Microchem) was spincoated at 700 rpm onto a silicon wafer, soft baked at 95°C for 10 minutes, and exposed with a 200 mJ/cm^2 dose at 365 nm using an EVG 620 mask aligner. After post-exposure bake at 95°C for 5 minutes, the exposed SU8 was developed with SU8 developer (Microchem) for 5 mins. The fabricated SU8 mold was placed in a Petri dish and treated with Trimethylchlorosilane (TMCS) vapor for 5 minutes to facilitate PDMS release. Then PDMS prepolymer (RTV 615, MG Chemicals) was mixed at A : B 10 : 1 ratio and degassed in a vacuum chamber. The degassed PDMS prepolymer was poured onto the SU8 mold and cured at 80°C for 30 mins. After PDMS was peeled off from the mold, inlet/outlet holes were punched through the whole layer with a 0.75 mm biopsy punch. Meanwhile, the 1.5 mm by 1.5 mm CMOS die was placed top side down on another polished 3 inch silicon wafer held in a Petri dish. A 23 gauge blunt needle was used to apply a 5 psi pressure on the back side of the CMOS die to prevent PDMS leakage under the die. Then pre-degassed PDMS prepolymer (RTV 615 10 : 1) was poured onto the die and baked on a hotplate at 90°C for 5 mins. Then the needle was retracted from the die and extra PDMS prepolymer was added to fill the Petri dish. After curing at 80°C for 30 mins, the CMOS layer was peeled off from the wafer. The microfluidic and CMOS layers were then both treated with air plasma (BD-20AC, Electro-Technic Products) for 15 s. Immediately after plasma treatment, the two layers were manually aligned and bonded under a 180X stereoscope (SM-2TZZ, AmScope). The bonded package was baked at 80°C for at least 8 hours. Finally, Galinstan was injected into the dedicated microfluidic channels at room temperature by hand pressing a 3 cc syringe to form the electrical interconnects.

I–V characterization of packaged CMOS transistors under stretching and bending conditions. The I–V characteristic of the NMOS transistors in a traditional DIP-40 package (Kyocera KD-78163 DIP-40 ceramic package) and the proposed flexible PDMS package were measured using a stable voltage source and two digital multimeters. Gauge 21 stainless steel tubes (Small Parts) were used to connect the liquid metal interconnects to the test equipments. For $I_{ds}-V_{ds}$ measurements, the gate voltage was set at fixed values (V_{gs} = 1.0 V, 1.5 V and 2.0 V) using a DC power supply (E3613A Agilent). The drain voltage V_{ds} was swept from 0 V to 1.4 V using the same power supply. The accurate readings of V_{ds} were recorded with a true RMS digital multimeter with a voltage resolution of 1 μV (Keithley 179). The drain currents I_{ds} were then measured with another digital multimeter with a current resolution of 1 nA (Keithley 179). During the stretching tests, the package was fixed to two linear translation stages (PT1 Thorlab) using PDMS as the glue. The I–V characteristics of the DIP packaged NMOS transistor was also verified by a semiconductor parameter analyzer (Agilent 4155C).

Magnetic nanoparticle detection with the packaged CMOS/microfluidic hybrid microsystem. A polarization magnetic field was applied by a Helmholtz coil (EM6723, Pasco Scientific) in the range of 1-60Gauss. A 10 kHz modulation of the magnetic field was generated by an AFG 3031B, Tektronix function generator. Magnetite Fe_3O_4 nanoparticle colloid solutions (Ferro-Tec EFH1, mean particle diameter of 10 nm) were used in the experiments. The readout circuit converted the small MAGFET current difference into a voltage difference, which was amplified by an Op-Amp circuit. The voltage output was sampled via an audio input line to MATLAB at a 9.6 Ms/s sampling rate. This signal was then transformed into the frequency domain using FFT's to find the signal amplitude at 10 kHz. The detection bandwidth was 10 Hz limited by the signal integration time.

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Author contributions

Z.Y.L. and M.E.Z. conceived the idea. B.W.Z., C.E.K. and M.E.Z. designed the CMOS chip. B.W.Z. designed the microfluidics layout with inputs from Z.Y.L.. Z.Y.L., B.W.Z. and Q.D. performed the fabrication, packaging and measurements. Z.Y.L., B.W.Z., C.E.K. and M.E.Z. wrote the paper. Z.Y.L., C.E.K. and M.E.Z. provided guidance.

Additional information

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